15 AND 30 VOLT REGULATOR – 100

The 15 and 30 volt regulator board supplies the signal processing circuitry with precisely regulated, low noise, low voltage supplies. The regulator topology is noteworthy in that it requires minimum "head-room" (wasted input voltage over that required to produce the desired output voltage) insuring maximum efficiency and minimum heat dissipation.

Most of the electronics are located on the integrated circuit(s) IC101/102. This device supplies a temperature-compensated, low-noise reference voltage, and contains a low-drift, high gain operational amplifier with an extra input for current limiting. Q1 supplies a constant current for zener diode D1 which is used to bias constant-current sources Q3, Q7 and Q8. Q4, Q5 and Q6 supply a temperature-compensated constant current for reference zener diode D2, and Q5 supplies the actual reference current. Q9 and Q10 function as a current repeater, supplying a stable bias voltage for current source Q13. The operational amplifier consists of differential pair Q11 and Q12, fed from current source Q13. Current source Q8 is the active load for Q12, providing for high voltage gain in this stage. Q14 and Q15 provide current gain; while D3 extends the range of possible output voltages down to below 0 volts. Q16 provides for current limiting; upon saturation, Q16 robs collector current from Q12, forcing the output low.

The 15 and 30 volt regulators are virtually identical, except for some additional components (R20, R21 and C6) which reduce the maximum input voltage to a safe level for the integrated circuit IC102. Considering the 15 volt regulator, a voltage from +17 to +25 volts (depending on line and load) is applied to pin 2, where it is by-passed by C1. While R4 feeds B+ to the IC, the main current path is from current-sensing resistor R2 through the external pass transistor to the output, pin 4, where it is decoupled by C4 and strapped to pin 6, (the regulator sense input). A certain fraction of the sense voltage, determined by R14, R15 and R16, is then applied to the inverting input of IC1 for comparison with the reference voltage, which is derived from IC1's internal reference voltage output. The reference voltage is divided by R8, R9 and filtered by C2 to reduce reference voltage noise and to allow the operational amplifier to operate over a favorable output range. Should the output voltage go high, the V_Z output of IC1 will go low, causing Q2 to pull less base current from the external pass transistor, which then reduces the output current and, hence, voltage. R1 both limits the amount of power dissipation in Q2 and protects the external transistor from excessive base current in the event of an overload, or excessively low line voltage.

During turn on, as the raw supply filter capacitors charge, IC1 supplies no base drive for Q2 because the B+ voltage supplied to it is insufficient to bring the V_Z output positive, so Q2 and the pass transistor are both off. At such time as V_Z goes positive, the output voltage is zero, and Q2 saturates, saturating Q3 and shorting the output voltage to the input voltage. (See Figure 100-1.) This situation continues until the input voltage exceeds the nominal output voltage, at which time, the circuit commences linear regulation.

Current limiting and foldback is provided by Q1. The current limit value is set by R2; if enough current passes through R2 to cause a voltage drop of .6 volts, then Q1 turns on, causing Q16 (on IC1) to saturate, forcing the V_Z terminal low, thereby reducing the base drive to Q2 and the pass transistor, and reducing the output voltage (and the output current). If the output is grossly overloaded or shorted, the output voltage will drop to zero, and R13 will increase Q1's base drive, which will reduce the amount of current necessary through R2 to keep Q1 on (Figure 100-2). Thus, the amount of output current is reduced (or "folded-back") to a value that is safe for the regulator.

The regulator is compensated by R10 and C3, which rolls off the high frequency response of the regulator. C4 supplies enough current to compensate for the necessarily reduced output slew rate, which otherwise would result in poor step response.

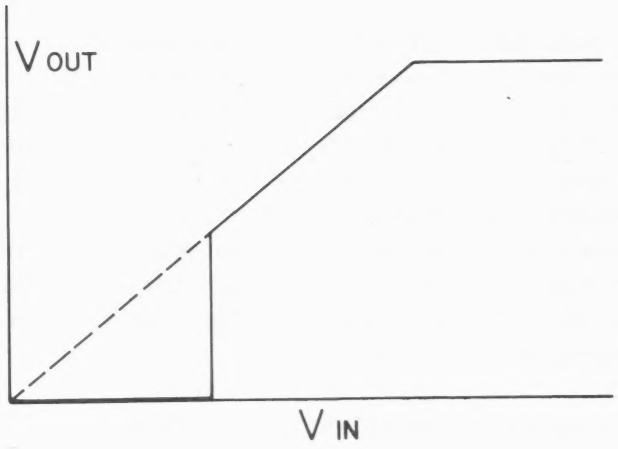

Figure 100-1

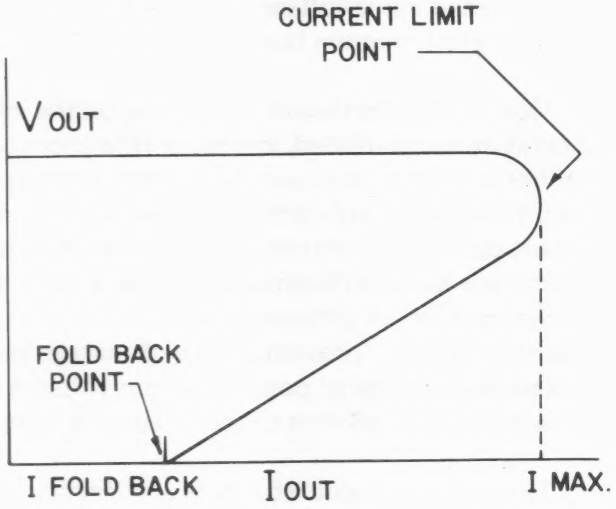

Figure 100-2

IF/AFT – 300

The IF strip accepts the intermediate frequency output from the VHF tuner and produces the baseband video signal and the 4.5 MHz FM sound signal. It also supplies an amplified IF signal to the automatic fine tuning (AFT) circuitry, which then applies corrections to the tuning voltage at the tuner.

The IF signal from the tuner is coupled by C1 to Q1, a common-base amplifier which transforms the impedance to 300 ohms while providing 12 dB of voltage gain. Q1 is feedback biased by the divider R5, R2, which is tied to the supply voltage at the R3, R4 junction. C2, C3, and R3 provide power supply bypassing and decoupling, while C4 AC bypasses the base; L1 is a DC bias return. The signal is coupled by C5 to the IF filter, which consists of nine resonant tanks: L5-L13 in conjunction with C11, 13 . . . C27, which are coupled by C12, 14 . . . C26. It provides extremely sharp rejection of out-of-band signals without the need of trap networks. The filter is terminated by R12 and the signal is coupled by C28 into IC1, an IF amplifier, whose gain is controlled by the AGC voltage. C29, C31, and C34 are bypass capacitors with R15 providing power supply decoupling. The amplified signal is developed across the tank L14-C33 which is swamped by R16; it is then coupled by C35 through R18 to IC2, the demodulator. The IF signal is buffered in the IC and appears at pin 1. The signal for the AFT passes through R19 and C36.

IC2 is a synchronous demodulator which multiplies the IF signal by the carrier, which is developed across the tank C39-L15, tuned to 45.75 MHz. The resultant baseband video signal appears at pin 4, where the sound subcarrier output is provided for the audio demodulator board. The sound subcarrier is then trapped from the video by sound trap C41, L16, R25, and the signal is buffered to the AGC/IF processor board (400) by 03.

The AFT circuitry consists of an integrated circuit amplifier-limiter and discriminator that measures the difference between the IF picture carrier frequency as tuned and 45.75 MHz, the correct frequency. Any difference results in a correction voltage that is used to change the frequency of the local oscillators in the UHF and VHF tuners.

Assuming Q8 is "off" the IF voltage is applied to an amplifier-limiter in IC3 at pin 12. The output of this amplifier is developed across the resonant circuit consisting of the primary of discriminator transformer T1 and C48. The secondary of the transformer, tuned to resonate with C52 at 45.75 MHz, feeds the discriminator network in IC3. The output of the chip is a differential voltage at pins 5 and 8: typical levels at each pin are 9V p-p, with zero deviation from 45.75 MHz resulting in 6.5V. For fine tuning the AFT can be defeated by a front panel switch which shorts the positive and negative outputs together. The AFT output voltage, buffered by Q10, acts to change the divider network R59-R60; in this way the voltage from the channel selectors is altered up or down to create the appropriate tuning voltage. For UHF operation it is necessary to reduce the sensitivity of the AFT circuitry, since the UHF tuner requires a smaller change in voltage to induce a given change in local oscillator frequency. Thus, when the UHF/VHF switch is in the UHF position, +24 volts is applied to R54, and Q11 is saturated: in this case R57 is tied to ground, and the sensitivity is reduced.

Q6-Q8 serve to interrupt the AFT operation both when the channel selector is between stations and also when the UHF/VHF switch is between contacts. This action is necessary to insure that the AFT doesn't lock onto an adjacent channel sound carrier when stations are being changed. Normally, Q8 is "off" as Q6 and Q7 are "off" and R44 pulls Q8's base towards -15V (until D6 clamps the base at -0.6V). However, if either Q6 or Q7 turns on then current (limited by R43) charges C46 until Q8 turns on and unbiases the input stage of IC3, defeating the AFT. Q6 is turned on whenever the UHF/VHF switch does

not supply +24V to R36 – in that case the divider R35, R36, R37 forward biases the base. Q7 is turned on whenever both JP 15-4 and JP 15-5 are open, i.e., when the channel selector is between stations. In that case current flows from +24 volts through R40, R41, and R42 to Q7's base.

Q5 in concert with the channel selector switch provides the VHF tuner band-switching voltage: -15V for low band (Ch's 2-6), +22V for high band (Ch's 7-13), and +22V during UHF operation. When the UHF/VHF switch is in the VHF position, +24 volts is applied to D2 and R38 is in parallel with R40, and is thus negligible. In this case Q5 is "on" when R41 is grounded (high band) and is "off" when R42 is grounded (low band). Thus, for high band Q5 is saturated and the band voltage equals +24 volts minus Q5's saturation voltage; otherwise, when Q5 is "off", R34 pulls the band voltage to -15. During UHF operation D2 is reverse biased and R38 and R39 forward-bias Q5, irrespective of the channel selector grounding action: thus the band voltage equals +22 volts.

Finally, Q9 acts as an emitter follower with a zener diode reference at the base to provide a regulated +24 volts.

AGC/IF PROCESSOR – 400

The AGC/IF processor board provides automatic gain control voltages for the IF strip and tuner in such a manner as to closely control the IF strip video output amplitude. A second section of the board provides base-band compensation such that the video signal delivered to the receiver is flat in amplitude and phase from DC to 4.1 MHz (-3 dB).

The IF video output stage is biased at 9.5V for zero carrier, which corresponds to a 120 Average Picture Level (APL) signal, +120 IRE (see Figure 400-1). Sync and shades of gray correspond to voltages which are negative with respect to this reference voltage. In order to insure a video output of 3.5V p-p (measured from -40 IRE to +100 IRE), it is necessary to adjust the gain of the tuner and IF amplifier such that the detected tips-of-sync voltage is 9.5V - (160/140) x 3.5 = 5.5V. The AGC processor insures that this condition is met by sampling the tips-of-sync voltage and adjusting the IF and front end gains.

Video is fed into pin 9, where it is applied via R22 to Q7. If the sync tips of the incoming signal fall below the reference voltage applied to Q7's emitter from the AGC control, then Q7 will turn on. As a result Q8 and Q9 turn on, and a 30V pulse appears across R29 and R30. R26, while providing some feedback, has the primary purpose of preventing Q7 from being reverse-biased if the connection to the IF strip is opened. The sync pulses appearing across R30 charge C17 through D4, creating a voltage that ranges from 0 to 20 volts. This voltage, divided by R31 and R32 and emitter-followed by Q10, controls the gain of an integrated circuit amplifier in the IF strip. The release time of this circuit is set by C17 and the parallel combination of R31-R32 and R34, R35, R36. Note that the AGC control, by setting the reference that the tips of sync are compared to, determines the peak-to-peak amplitude of the video signal.

The tuner requires a positive voltage of 10V for maximum gain, with gain reduction occurring with less positive voltages. R34, R35, and R36 provide a sample of the IF AGC voltage which is fed to Q11's base. During weak signal conditions, the IF AGC voltage is low enough for Q11 to become forward-biased and consequently saturated, which clamps the RF AGC voltage to about 8.6 volts. As the RF input signal is increased, the IF AGC voltage increases until Q11 comes out of saturation, and the RF AGC voltage is pulled down toward a negative voltage, decreasing the front end gain. At some point, no further gain reduction is possible in the front end, and the IF AGC voltage once again increases, leaving the RF AGC voltage at its minimum value. (See Figure 400-2.)

The input video is also applied to amplifier Q1, which serves to equalize the amplitude response of the signal from the IF strip. This is accomplished by peaking the response of the common-emitter stage at three separate frequencies determined by the three series resonant LC circuits at Q1's emitter. The output of this stage, flat in amplitude, appears at Q1's collector across R5 and R6.

Q2, Q3, and Q4 are stages that serve to alter the phase characteristics of the signal while maintaining flat amplitude response. (Since each functions identically, only that stage involving Q3 will be discussed.) Above and below the resonant frequency of L4 and C9 all the current from Q2 flows through R10, R11, and D1. The resultant voltage across R11 and D1 is emitter-followed by Q3 to create a current across R14. Thus, outside resonance the output current from Q3 has the same amplitude as the input current and is in phase with the input current. However, at resonance the current from Q2 flows through L4 and C9 to Q3 acting as a common base amplifier. Thus, in this case the output current equals the input current in amplitude but is shifted 180°. Around resonance the action of the circuit is such that the amplitude of the output current is equal to the amplitude of the input current while the phase shift varies from 0° to 180°

below resonance and from 180° to 360° above resonance. Thus Q2, Q3, and Q4, acting at frequencies determined by L2-C5, L4-C9, and L5-C10, serve to equalize the phase response of the signal from the IF strip.

The result of Q2, Q3, and Q4's action is a current from Q4 that is converted to a voltage by R16. This signal is buffered to the receiver by emitter-follower Q5. Q6 provides an even lower impedance in order to feed the 75Ω output, source-terminated by R21 and amplitude-controlled by R18.

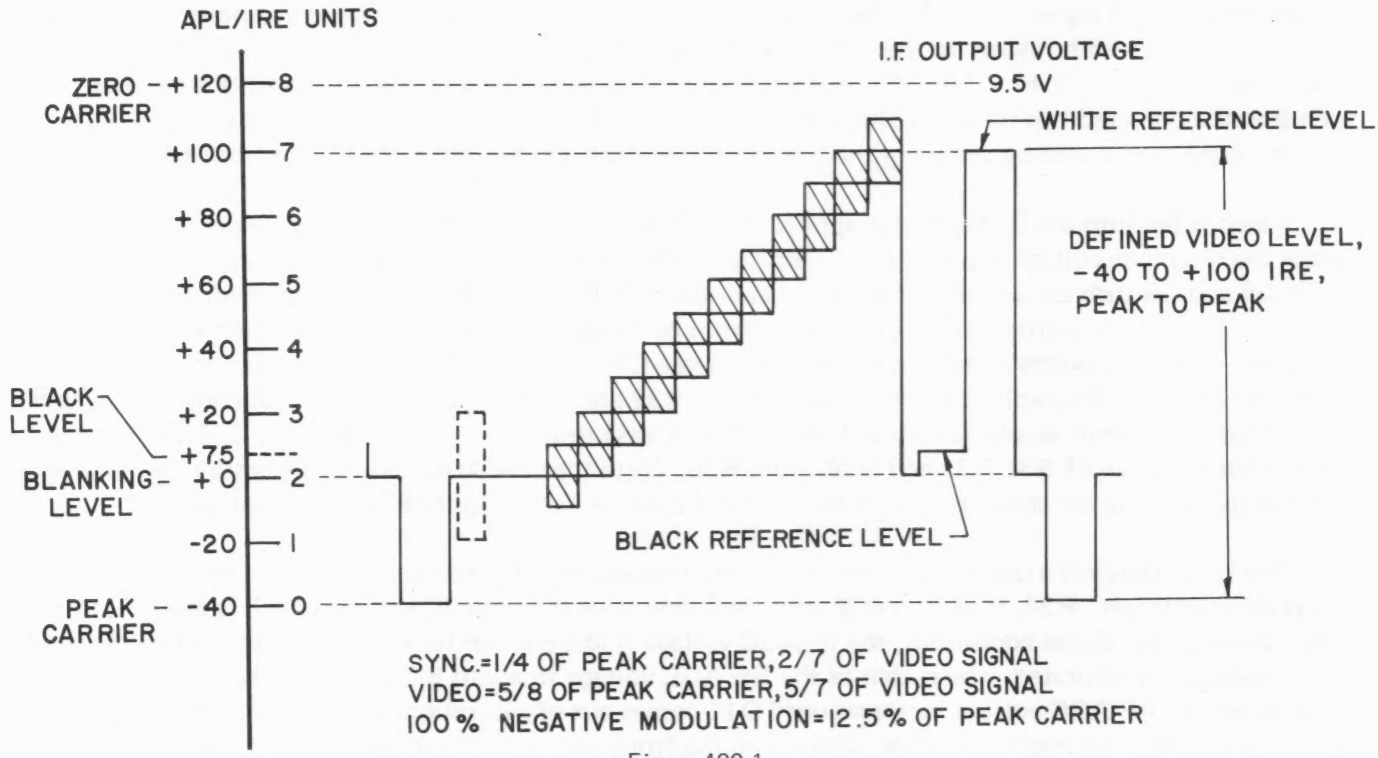

Figure 400-1

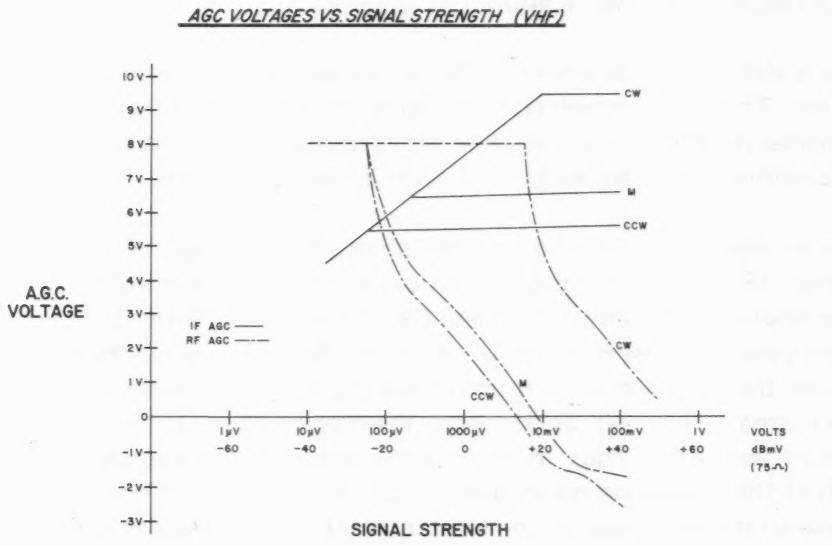

Figure 400-2

(CCW, MIDRANGE, CW-REFERS TO POSITIONS OF RF AGC DELAY POT)

AUDIO DEMODULATOR BOARD – 500

The 4.5 MHz FM aural signal from the IF Assembly drives a ceramic filter which provides bandpass shaping to exclude unwanted frequencies. After filtering, the signal is passed to IC-1 which provides IF amplification, limiting, and detection. Quadrature detection is used, and only one adjustment is necessary. The detector is aligned by tuning inductor L1 for maximum recovered audio with minimum sync buzz at TP3. A 1 KHz, 100% modulated signal should provide about 1.5V p-p at TP3. Capacitor C8 provides deemphasis to compensate for the preemphasis boost used in transmission.

Q1-3 form an audio amplifier to boost the output of the detector to levels used to feed external outputs and the volume control. TP3 and TP4 should be biased at 7.5 Vdc. The 1 KHz, 100% modulated signal should produce about 5.5V p-p at pin 11 and 1.3V p-p at pin 12.

Q4 is an emitter follower which is used to provide an isolated high impedance input for external audio sources. TP5 should be biased at about +7 Vdc. The output of the emitter follower drives the "External" position of the NORM-EXT switch.

TONE CONTROL – 600

The tone control assembly operates in conjunction with active equalization in the power amplifier to compensate for the speaker location and program quality differences.

The tone control assembly is a treble shelf control with a range of +4 to -8 dB at 10 kHz. Transistor Q1 operates as a unity gain phase splitter. Signals arriving at Q1's base are in phase at the emitter and out of phase at the collector. The tone control action is caused by capacitor C5 which is applied between the emitter and ground (causing high frequency boosting) or between the collector and ground (causing high frequency attenuation) by varying R8.

AUDIO POWER AMPLIFIER - 700

The audio power amplifier amplifies an audio signal from the volume control and drives the 8Ω speaker.

The input stage is a differential amplifier, consisting of Q1, Q2 and constant-current source Q6. The input signal is AC-coupled through C1, given high-frequency rolloff by R3 and C2, and drives Q1, which in turn drives voltage amplifier Q3. Current for Q3's collector is supplied by constant-current source Q7 which provides a very high impedance load for Q3, giving Q3 a very large voltage gain. C9 gives the amplifier single-pole open loop response, thus insuring closed loop stability. Current gain is provided by Q4, Q8, Q5 and Q9. D2, D3 and D4 provide bias and temperature compensation for the V_{be}'s of the current amplifier and with R10 insure a stable voltage drop from Q5's emitter through R13 and R14 to Q9's emitter. Thus, quiescent current through Q5 and Q9 is well controlled. The output stage provides Class B amplification at large signal levels, (although Q5 and Q9 may enter cutoff during portions of an output cycle). The output is fed back to Q2 via an equalization network of R9, R7, R6, R5, C8 and C6, providing bass and treble boost to compensate for speaker characteristics. C7 provides an AC ground return path and DC blocking, to allow for 100% DC feedback.

Of the power supplies, only +15V is tightly regulated, while the nominal -8.5V and 23V supplies are subject to ripple, and the 23V supply is completely unregulated. DC bias for Q1's base (approximately +5V) is provided by the stable +15V and network of R1, R15, R16, D5 and D6 ultimately connecting to -8.5V. Ripple that might propagate from the -8.5V supply to Q1's base is shunted to ground through C3. The voltage drop across D5 and D6 provides a bias for constant current sources Q6 and Q7. C4 reduces ripple voltage across R16, D5 and D6, thus reducing ripple modulation of the current sources.

After power turn on, C4 would charge relatively slowly, causing a delayed turn-on of Q6 and Q7. C10 provides a current pulse through D7 and R18 during turn-on, thus quickly turning on Q6 and Q7. After power turn-on, R19 pulls the top of C10 down to -8.5V, causing D7 to reverse bias, disconnecting the circuit. A similar rapid turn-on is provided by the feedback path from the output (Pin 1) through C5 and D1. This prevents a large positive output transient during turn-on. As C7 charges, normal bias feedback is established, and R8 discharges C5, sending D1 into cutoff.

EXTERNAL VIDEO AMPLIFIER - 800

The external video amplifier board accepts a 1 volt peak-to-peak, standard composite NTSC video signal and amplifies it to 3V p-p, while removing interference such as R.F. from nearby A.M. radio stations or 60 Hz ground-loop hum which may develop between two pieces of equipment separated by a large distance or plugged into different AC power outlets. The board passes the differential-mode signal and rejects the common-mode interference.

The video comes into pins #3 and #4 of the board. Pin #3 is connected to the shield of the input connector and pin #4 is connected to the center conductor. The co-axial input is terminated by R12 (75 ohms) while C6 bypasses high-frequency noise. C5 and C7 are DC blocking capacitors. The base of Q4 is held at a DC potential of 15 volts, determined by R2 and R15. The AC signal on the shield is coupled to the base of Q4, and consequently, appears on the emitter of Q4. D2 and D3 provide transient protection.

The actual video signal is the difference in voltage between pins #3 and #4. This voltage signal is turned into a current signal by R13, and is then injected into the emitter of Q4 and re-appears at the collector of Q4 and into R16 where it is converted back into a voltage. The gain of the input stage is the ratio of R16 and R13, (1/3) so a video signal of 1/3V p-p is developed across R16. The common-mode interfering signal appears equally on the shield and center conductor, so there is no voltage developed across R13 and consequently, no current injected into Q4 and R16.

Q1 serves as a constant-current source which delivers a 1 ma current to bias Q4 and the later stages of the amplifier. C8 and C9 form a pre-emphasis-de-emphasis network which swamps out Q4's base-to-emitter capacitance, assuring that the overall response of the amplifier is flat to 5 MHz.

Q5 and Q2 comprise a simple two-stage amplifier with variable feedback in the emitter of Q5. The gain of the amplifier is set by the value of R18: amplifier gain is the ratio of R19 to R17 and R18, and can be adjusted for a minimum gain of 6 to a maximum of 12 (2X to 4X overall). Proper adjustment of R18 results in a video signal of 3V p-p on the collector of Q2, which is then buffered by the emitter follower Q6, and then fed into C12. C12, Q3 and its associated components, D1 and R21 form a sync-tip clamp circuit. The purpose of the clamp is to remove any last traces of hum or low-frequency disturbance which may be present on the video signal. The clamp works by changing the voltage across C12 such that the tips of sync are clamped to a fixed voltage (nominally 6 volts). During a line, R21 charges C12, increasing the voltage across C12 (by a amall amount) and thus lowering the DC component of the video signal toward ground. However, the signal can never go more negative than the voltage determined by R10 and R9 (buffered by Q3 and decoupled during the video portion of the line by D1). During the horizontal and vertical sync pulses the voltage at the base of Q7 is held clamped, and C12 is partially discharged. Consequently, any base-line disturbances such as hum or poor low-frequency response (tilt) in preceding equipment are removed.

Q7 acts as an emitter follower, providing an impedance transformation between the high-Z clamp circuit and the output.

The gain adjustment, R18, is set by feeding in a 75 ohm composite NTSC video signal of 1V p-p and adjusting R18 such that the output amplitude is 3V p-p.

COMB FILTER - 900

The comb filter board accepts a 3V p-p composite NTSC video signal and from it derives a full 4.1 MHz bandwidth luminance signal and a full 1.5 MHz bandwidth chrominance signal. Moreover, in addition to recovering the complete bandwidth of the two signals, the board, depending upon the nature of the composite input signal, produces a luminance signal with no chrominance in it and vice-versa.

The name "comb filter" is descriptive of the process used to recover the chrominance and luminance signals from composite NTSC video. If it is assumed that the video signal is unchanged from line to line and hence periodic, then it follows that the luminance information is grouped at discrete intervals in the frequency spectrum, namely at whole multiples of 15.75 kHz. Moreover, the chrominance information is also grouped at these intervals. Thus, by choosing a color subcarrier frequency equal to an odd multiple of one-half the line rate (3.58 MHz = 455 X 15750/2), the chrominance information will be centered in the gaps of the frequency spectrum left by the luminance information. This method of combining the two signals is known as "interleaving"; as a result it is possible to recover the pure luminance and pure chrominance signals by using a filter with a response shaped like a comb, i.e., pass (or stop) bands every 15.75 kHz. This recovery is actually accomplished by noting that, due to the relationships required for interleaving, the chrominance signal is out of phase in any two consecutive identical lines, while the luminance signal is in phase line-to-line. Thus, adding two consecutive lines gives pure luminance, while subtracting them gives pure chrominance. In the comb filter board, the video signal is delayed one line and then subtracted from the next line, producing chrominance. The luminance is recovered by subtracting the chrominance from the composite second line.

The 3V p-p composite signal at pin 1 is coupled by R13 and C10 to Q3, an emitter follower. This transistor drives the delay line, the circuit where subtraction with the previous line takes place (Q11, Q14, Q15), and also the circuit where the chrominance is subtracted from the composite signal to produce the luminance (Q12, Q16-19). Note, however, that the DC path for Q3's quiescent current (approximately 10 ma.) is R16, R17, Q6, R33, R34, and Q9. R16 (and R22 on the output side) provides the resistive termination for the delay line. However, the delay line, which is a mechanical delay line using piezoelectric transducers, has fairly large parasitic capacitances associated both with the input and with the output. In order to maximize the transfer of energy, circuits which effectively create negative capacitance are in parallel both with the input (Q6, Q9, and associated components) and with the output (Q7, Q10). (In the analysis to follow all statements about the input apply similarly to the output.) The voltage at the input of the delay line causes a certain amount of current to flow into the stray capacitance of the input. To cancel the effect of this capacitance it is necessary to have a current equal to that current flow from Q6 and R17. This is accomplished by taking the voltage at the input of the delay line and coupling it via R17 and C19 to the base of Q9. Since the voltage on Q6's base (and hence the top of C17) is fixed at AC ground, the varying voltage on Q9's emitter causes the necessary current to flow in C17 and hence through common base amplifier Q6.

As the signal passes through the delay line it is band limited by the line itself to approximately .5 MHz above and below 3.58 MHz. Further shaping of the amplitude and phase characteristics of the signal is accomplished by C12, C13, C23, C24, L3, L4, L5, and associated resistors; Q4 and Q5 are common base amplifiers, while Q8 is an emitter follower. The resultant composite, band-limited, one line delayed signal is applied to Q14, a common emitter stage, where R58 provides gain adjustment.

At the same time the following line of video is being buffered by Q3 to R64, where R64 works against C32 to high-pass filter and consequently match in phase and amplitude this signal to that on Q14's base. Thus R64 functions as a phase adjustment for complete subtraction of the two lines. The voltage shaped by R64-C32 creates a current which passes through common base amplifier Q15, is further shaped by L7 and C30, and is current summed in Q11 with the current created by Q14. Since there is a 180° phase shift in common emitter stage Q14, the two signals are actually being subtracted. The result of the subtraction process is the desired chrominance signal, which appears as a voltage across R45. This voltage is low-end band limited by L6-C27 and emitter followed by Q13. Finally, the variable chrominance signal is made available at pin 12 after passing through common base amp Q21 and emitter follower Q22.

The remaining step is to recover the luminance by subtracting the chrominance signal from the composite signal. This process takes place, again as current addition of out-of-phase signals, in Q19. The chrominance signal at Q13's emitter is coupled by C28 to C33 and L9. C33-R60 provide approximately 90° phase lead, which brings the chrominance signal 180° out-of-phase with the luminance signal to which it is added in Q19. Q18 serves to isolate L9, which shunts low frequencies from the signal path, from any voltage appearing on Q19's emitter. Meanwhile, the composite video from Q3 is low-pass filtered by R64-C32 and applied to common emitter stage Q12. Common base amplifier Q16 serves to isolate phase compensation networks L8-C31 and L11-C36. Finally, this voltage, applied to Q17's base is converted to a current for current addition in Q19; the result is the luminance signal converted to a voltage across load R54 and buffered to pin 10 by emitter follower Q20.

COMB FILTER – 900 – REV 7,8

The Comb filter board accepts a 3 volt peak-to-peak composite NTSC color signal and separates the signal into a luminance (black and white) signal and a chrominance (color difference) signal. This separation is performed in essentially the same manner as in previous revisions of this board.

In terms of signal processing stages, Q1 is the input buffer amplifier; Q2, Q3, Q5 and Q6 form two negative capacitor simulators to aid in matching the delay line; Q4, Q7, Q8 and Q9 provide some voltage gain while equalizing the frequency and phase response of the delayed signal. Q10 and Q11 provide a variable amount of delay for the composite signal, which is split, with a portion of the signal going to Q13 and into the subtraction circuit consisting of Q13, Q12 and Q14. The combed chrominance signal is taken from the emitter of Q14, and feed to the high-pass stage Q16. The subtraction of the chroma from the composite occurs at the base of Q17, with the combed luminance signal taken from Q17's emitter.

The Quartz delay line is excited by piezo-electric transducers, which exhibit about 140 p.f. of reactive impedance. Because real power is coupled into the line and must be absorbed at the source and load, this reactive impedance must be cancelled by a reactive impedance of opposite sign. This impedance could be provided by an inductor, but the value would be correct at only one frequency. Instead, the correct value of positive reactance is provided with a "negative capacitor." The voltage on the terminals of the delay line is fed into Q3 by C5. The voltage on Q3's emitter causes a current to flow through C2 (Q2's emitter is at AC ground) and into Q2's emitter; this same current must flow out of Q2's collector and consequently from the delay line terminal. The circuit acts like a negative capacitor because, if a positive-going voltage transition is applied to a capacitor, it draws a positive spike of current; however, positive-going voltage transitions on Q2's collector result in negative-going spikes of current.

Thus the delay line is matched by the terminating resistors, R4 and R20, and by the negative capacitors. The one-line-delayed signal is then processed by an all-pass filter stage consisting of Q4 and Q7. Q4 is a common-base amplifier (current follower). Common base amplifiers have their base AC grounded, which forces the emitter to also be at AC ground. Because the transistor is biased in its active region, any current that is injected into the emitter of the transistor must come out of the collector. Since this signal current must flow from the collector regardless of the voltage on the collector, the transistor acts as a high-impedance current source, which is useful for feeding many types of filters. Q4 feeds an all-pass filter consisting of Q7, L9, C7 and associated resistors. At frequencies far away from the resonance on C7 and L9, most of the current from Q4 flows into R14 and R13. Q7 takes the voltage signal produced across R13 and outputs a current approximately equal in magnitude but opposite in phase to that flowing out of Q4. At frequencies near or at resonance, L9 and C7 present a low shunt impedance to Q7's emitter (which, because the current from Q4 is not flowing to R13, is effectively at AC ground) and inject current into Q7 which must also exit via Q7's collector but in phase with the current from Q4. So, while the magnitude of the current from Q7 does not change with frequency, the phase of the current goes from +180 degrees at low frequencies, through 0 degrees at resonance, and on to -180 degrees at high frequencies. Some of the frequency response equalization occurs in the two L-C filter stages prior to

Q8, which is an emitter follower. Q9 is a common emitter stage which is used to provide gain to make up for signal losses in the delay line and the filters. The L-C filter stage coupling Q9 to Q12 forms a combination high-pass and band-reject filter (the band reject filter is made very gentle by shunt resistor R39). The current that is injected into the emitter of Q12 then flows into R41, where it is mixed with signal current from the undelayed line, provided by Q13. R52 subtracts a certain amount of DC current from Q12, allowing Q9 to run at a high level of quiescent current (necessary for low signal distortion). The voltage across R41 is the difference between the current line and the delayed line, which is the chroma signal. Emitter follower Q14 buffers the chroma signal both to the output pin and also into the chroma subtraction stages. R55 provides DC feedback to the negative capacitor circuit Q5-Q6.

The composite input signal is transformed into a current by Q10, and fed into a first-order all-pass filter consisting of Q11, L3 and associated resistors. The function of this circuit is similar to the Q7 stage, except that instead of an L-C resonant circuit, only an inductor is used. The phase of the output current from Q11's collector goes from 0 degrees at low frequencies to -180 degrees at high frequencies. This output current is split by C20, L6-C24 and R46, with the high frequencies fed into common base stage Q13 and then into the subtraction circuit. The remainder of Q11's collector current flows into the Q15 base circuit, developing a voltage which is then transformed into a current by Q15. This current flows into a further stage of low pass filtering and then into R49.

The action of the low pass filters upon the composite signal is quite gentle and does not affect the luminance components up to about 4.2 MHz, except by introducing a certain small amount of time delay to compensate for that incurred in the chroma combing process. The combed chrominance signal is fed via C23 to Q16, which serves to high pass filter the chroma signal in order to remove low frequency interference caused by spurious reflections in the delay line. The filtered chroma is then injected into R49, where it cancels the chrominance present in the composite signal, leaving a luminance signal. Q17 buffers this combed luminance signal to the output.

LUMINANCE PROCESSOR - 1000

The luminance processor board contains two separate circuits, the luminance processor and the sync processor. The first drives the delay line with the normal luminance signal, while the second accepts a luminance signal and from it produces four pulses that are used for timing, gating, and clamping throughout the receiver.

The 3V p-p signal at pin 6 is coupled by C6 to R8, where it is emitter - followed by Q2 to create a current in R12. Except for a fraction that flows through R3 and Q2, this current comes from +30V through Q3, R32, and L1. Thus the output voltage of the amplifier is slightly more than twice the input voltage, and a 6V p-p signal appears at TP 3. L1 provides an amplitude response boost of approximately 6 dB at 4 MHz to compensate for delay line losses, while R13 increases the DC bias current flowing in Q3. R10 provides the proper impedance match for the delay line.

In the sync processor section, R19, R23, R24, C8, C9, D3 and Q4 act as a sync separator. The base-emitter junction of Q4 working against C8 forms a clamp circuit that permits no part of a line to go below +30V minus the Vbe drop of the transistor. Thus negative tips of sync are clamped to approximately 30V; this clamping action charges C8 through R19 and Q4. The charging current is base current for Q4, and Q4 consequently saturates, producing a 30V pulse across R25. During the video portion of a line the base of Q4 is driven positive and Q4 is cut off; in this interval R24 discharges C8 towards ground. During the vertical interval Q4 must be held on for a longer period of time, and this time constant is supplied by C9 and R23. Thus, the pulses appearing at TP 6 are 30V pulses of approximately 4.5 μsec duration, coincident with the sync pulses of the video at pin 9. (See Figure 1000-1). These pulses are then buffered to pin 10 by Q10 and Q11.

The pulses at TP 6 charge C12 through R20. After approximately 4.5 μsec, the voltage on C12 reaches 9V (the voltage on Q5's emitter plus two Vbe drops) and Q5 turns on. Q5 and Q6 form a one-shot, and consequently a 30V pulse appears across R22. Q8 is an emitter follower that provides a low impedance output when the one-shot is off, while D7 conducts when the one-shot has fired. Positive feedback for the one-shot is provided by R14, C10, and D6, while D5 prevents Q5 from being driven too hard into saturation. The result of C12 and Q5-Q6's action is a pulse at pin 12 that is delayed 4 μsec from the start of the sync pulse, i.e., a pulse coincident with the back porch of the input video signal.

As the sync pulse at TP 6 goes high, C14 is charged through R30. When the voltage on C14 reaches approximately 5.5V, Q9 turns on and saturates, and consequently pin 11 is held low. Only after C14 discharges through R28 can the pulse at Q8's emitter drive pin 11 high. Thus the back porch clamp pulse, which otherwise would be the same as the burst gate pulse, is limited to about 3 μsec. This limiting locates the pulse approximately in the middle of the back porch when the pulse is used with video delayed 800 nsec by the delay line.

The sync pulses at pin 10 also drive current through R27, saturating Q7; this action holds pin 8 low. However, as L2 begins to draw current away from Q7's base, Q7 turns off, and Q10 drives pin 8 high, creating the sync clamp pulse. Since this pulse turns off when the sync pulse turns off, the result is a pulse that rises approximately 1 μsec after the sync pulse, and falls at the same time. The reason for this delay is so that the sync clamp pulse will be coincident with the sync interval of video that has been delayed 800 nsec by the delay line.

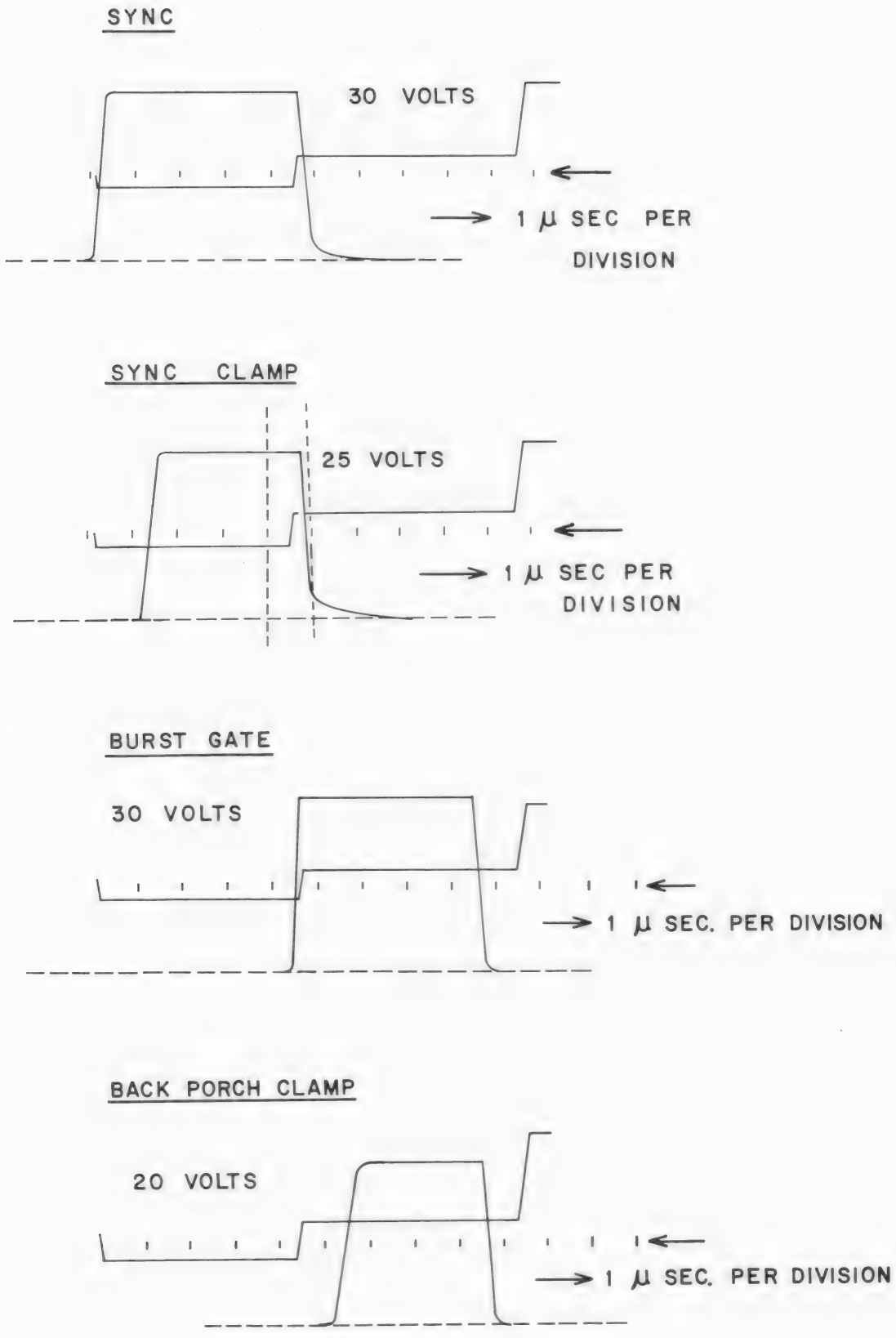

Figure 1000-1

CHROMA SYSTEM - 1100

The Chroma System serves two main purposes: It accepts from the Comb Filter (900) the chrominance portion of the composite NTSC signal and amplifies it; and it regenerates the color subcarrier, locked in phase and frequency to the color burst, for subsequent demodulation of the chrominance signal at the NTSC decoder board (1200). The board features circuitry that provides two separate time constants for both the Automatic Phase Control (APC) and the Automatic Color Control (ACC) feedback loops. When these loops are locked, a longer time constant is used for a low noise bandwidth, while out-of-lock a shorter time constant creates a greater pull-in range.

The chrominance signal on pin 7 is first applied to a high-pass filter consisting of R11, R12, L2, L3, C35, and C10. This is a fairly broad, essentially linear-phase filter whose function is to reject any information outside the chroma band (2.0 - 4.5 MHz). The signal is then AC-coupled by C11 to IC1, where it modulates current source Q1. The current from Q1 is divided in differential pair Q2-Q3 in a ratio determined by the ACC voltage supplied by IC2 to pins 1 and 14. The current that flows through Q3 develops a signal voltage across R5 that is buffered to pin 6 by Q6. The amplitude of this output is held constant for various chroma signal strengths by the action of the ACC loop. For example, as the amplitude at pin 6 increases, the differential voltage at pin 1 and 14 directs more signal current from Q1 into Q2 and less into Q3, thus reducing the output amplitude. As the input signal level falls the voltage at Q2's collector rises, and at a point determined by the Color Killer control (Q2's collector load) Q12 is turned on; consequently, Q13 turns off and Q14 turns on, and the second chroma stage is turned off. This action insures that during predetermined conditions of weak or black and white signals the set will operate only in monochrome, avoiding objectionable color noise.

The output of the first chroma stage is divided by R13 and R14 and then coupled back to IC1 by C12. The second chroma stage also uses a modulated current source (Q8), with the signal appearing across R8 being buffered by Q10 to the output. The gain of the stage (and hence the level of the chrominance signal) is controlled by a DC bias derived from the Color control on D2, which enters conduction and diverts current from Q9 and R8. The resultant chrominance signal is applied to common-base amplifier Q1, the output of which is peaked by L1, R9 and C7 at approximately 1.5 MHz to compensate for the low-end roll-off of the input filter at pin 7. Finally, Q2 buffers the signal out to pin 1. Note that the DC bias for Q1 is derived from the signal voltage; thus C6 is required in order to bypass the AC information.

IC2 both phase and frequency locks a 3.58 MHz oscillator to the color burst and also generates the ACC voltage for IC1. Locking of the oscillator is accomplished through the action of a phase-locked loop (PLL). Q1 and Q2 form the oscillator with a quartz crystal in series resonance in the feedback loop from Q2's collector to Q1's base, buffered from pin 6 by Q3. The oscillator frequency is determined by controlling the phase shift in the feedback loop. This shift is varied by the APC voltage on pins 11 and 12, developed from quadrature phase detector Q9-Q10, which determines how the current from Q2 is divided in differential pair Q5-Q6. Detector Q9-Q10 is a multiplier which compares the first chroma stage output, shifted approximately 90° by C19, R32, and L6, to the oscillator output. R37 provides a DC voltage that is converted to a current by R38 for injection into the detector; with P2-J3 open, R37 is used to adjust the free-running oscillator frequency. The ACC voltage at pins 15 and 16 is developed in a similar manner by Q15 and Q16. However, since the output of the first chroma amplifier is high-pass filtered by C18, R31, and L5 without appreciable phase shift, Q15-Q16 are an in-phase detector whose differential output signal is a function of burst amplitude. R36, R35, and C22 serve to inject a

DC current into the ACC detector - thus R36 controls the amplitude of the signal from the first chroma stage. R20 provides an offset for the ACC detector; when this offset is removed and pins 1 and 14 of IC2 are shorted by P1-J2, the chroma signal increases approximately 11 dB. Both the ACC and the APC detectors function only during the burst interval due to the action of Q19 (explained later).

As mentioned, the ACC and the APC loops have two separate time constants associated with them. When the APC loop is locked both Q7 and Q3 are "on", and C20 and C16 are connected across the APC and ACC correction voltages. However, when the APC loop is out-of-lock Q7 and Q3 are off, and the shorter time constants are created by R21 and Q7's "off" resistance in series with the capacitors. The switching of the two field-effect transistors is accomplished by Q5 and Q6. When the chroma system is locked, the DC voltage at pin 6 of IC1 is approximately 23V; in this case D1 is reverse biased, Q5 and Q6 are "off", and the voltage at point B is high. However, when the burst and 3.58 MHz oscillator are out-of-lock the DC voltage across R13 and R14 is 12V, and consequently current through D1 turns on Q5. As a result Q6 turns on and pulls current through D4 and D5, turning off Q3 and Q7. When the system passes from an out-of-lock to a locked condition, and Q5 turns off, base drive continues to be supplied to Q6 by C14 and D3. This action insures that while the voltage at point B can fall rapidly as Q6 turns on, it can only rise slowly as a ramp function.

Current from Q1 of the 3.58 MHz oscillator on IC2 normally flows to differential pair Q13-Q14. The output of these transistors is developed across collector loads L7 and R45, where the voltage across L7 is filtered of harmonic distortion by L9 and C31 and appears as a 2V p-p signal at pin 17. The Tint control provides a DC voltage which determines the relative amount of conduction between Q13 and Q14. With the phase shift network L8, C32, and C33 between Q13 and Q14's collectors, this difference in conduction changes the phase of the oscillator output.

The burst gate pulse applied to pin 15 performs two functions. First, the pulse saturates Q4, and as a consequence the 3.58 MHz burst is gated out of the chrominance signal. This action improves the demodulation that occurs on the NTSC decoder board. Second, in IC2 the pulse gates the current from the 3.58 MHz oscillator. Normally, Q19 of IC2 is off and the oscillator current from Q1 flows to Q13 and Q14. However, during the color burst the burst gate pulse saturates Q19 and consequently Q13 and Q14 are reverse biased. In this case the oscillator current goes to the APC and the ACC detectors for comparison with the color burst. However, to improve the demodulation in IC1201 it is necessary to have the oscillator current flow continuously to pin 17 of the chroma board. Thus, the oscillator current that flows to the two detectors during the burst interval is bypassed by C26, C27, C24, and C25 to common-base amplifier Q8, where it is added to the 3.58 MHz output.

NTSC DECODER – 1200

The purpose of the NTSC decoder board is to derive from the luminance and chrominance signals the red, blue, and green signals for the individual cathode-ray tubes. This is accomplished by first demodulating the chrominance signal to obtain the I and Q color signals and then by matrixing the I and Q voltages with the luminance (Y) to obtain R, B, and G.

The chroma signal coupled to pins 3 and 4 of IC1 is a 3.58 MHz subcarrier amplitude-modulated by color signals I and Q, which are in quadrature. In the IC this signal is applied to differential pairs Q15-Q16 and Q17-Q18, which convert the voltage into a current that flows into differential pairs Q5-6, Q7-8, Q9-10, and Q11-12. These differential pairs are switched on and off by the 3.58 MHz reference signals at pins 6 and 7 of IC1. The resulting multiplication creates sum and difference frequencies, and the difference frequencies buffered to pins 11 and 13 are precisely those signals that modulate the subcarrier, namely I and Q. The accuracy of this doubly-balanced demodulation depends upon the phase of the reference inputs, and L1 and C4 provide a variable, approximately 90° phase shift for the Q reference with respect to the I reference. Pin 9 of IC1 is a signal obtained by matrixing the I and Q outputs. R3, R4, and R7 provide terminations for emitter followers Q1, Q2, and Q3 of the IC.

The reason for decoding along the I and Q axes instead of decoding to obtain the standard (R-Y) and (B-Y) color-difference signals is that very precise band limiting can then be applied to the color signals as broadcast; this type of filtering is necessary to take advantage of the full 1.5 MHz bandwidth of the I signal that the comb filter board (900) provides. Thus L2, L3, C15, and R14 function as a 500 kHz low-pass filter for the Q signal, while L4, L5, C12, C14, and R19 are a 1.5 MHz low-pass filter for I. The I filter, consisting of Q1, Q3, Q6 and associated components, is more complicated for several reasons. First, since the I signal is transmitted as a vestigial side band (as opposed to Q, which is double side band), in order to recover a flat amplitude response it is necessary to have a filter with a response peaked at the high end (the region where I is single side band). Second, in order to equalize the group delays of two signals passing through filters with different bandwidths, it is necessary to add group delay to the wider bandwidth filter. Both of these additional requirements are met by Q1 and Q3. Q1 feeds I both through C8 to common emitter amplifier Q3 and also through L7 and R13. Q3 is biased to ground at the emitter by L6 in order to obtain the maximum drive capability at the collector. The inverted signal across R11 is then passed through C11 and added to the non-inverted signal from L7 and R13. This configuration creates the filter characteristics necessary to match I in phase and amplitude to Q.

The signal at pin 9 of IC1 is low-pass filtered by R8 and C9 to create an average reference voltage that reflects any drift in the I or Q outputs of IC1. This reference, buffered by Q5, is used throughout the NTSC decoder board as an AC ground and DC reference. For example, R14 is connected to AC ground to terminate the low-pass filter, while at the same time DC current is prevented from flowing through L2 and L3 and creating an offset.

The ≈3V p-p luminance signal at pin 18 appears across R23, which is the termination for the delay line. Q7 is an emitter follower that feeds the luminance to sync tip clamp capacitor C17. During sync intervals Q8 turns on, effectively shorting C17 and R31 to C18 and rapidly charging or discharging C17. In this manner the tips of sync are clamped to the voltage on C18, nominally 21V. The clamped video is then buffered by Q9 to the matrix circuitry.

Q10, Q12, and Q14 allow I, Q, and Y to be added in order to produce the R, B, and G voltages across R41, R49, and R58 respectively. For example, in each matrix the Y component creates a current across the 2K2 emitter resistor (R40, R48, R57) to an AC ground at the emitters of Q10, Q12, and Q14. This current passes through the transistors acting as common base amplifiers and then flows through the collector 2K2's, creating a voltage across R41, R49, and R58 equal (if R40 = R41, etc.) to that at TP 14. Thus in the equations for R, B, and G in terms of I, Q, and Y, the factor for Y in each case is 1. A similar analysis applies where I and Q are connected by resistors to the emitters of Q12 and Q14. In the base circuitry of Q10 and Q12, the contribution of each component is found by determining the signal voltage at the base and then by considering the respective transistor as a common emitter amplifier. Note that for R and G, R36 and R54 are phase controls, while R38 and R55 are amplitude controls. In the B matrix R46 affects both phase and amplitude.

Each matrixed output is buffered by an emitter follower, while R43, R51, and R60 protect these transistors from shorts at the output pins.

RGB PROCESSOR – 1300

The RGB processor board takes the red, green, and blue signals from the NTSC decoder board (1200) and amplifies them by a variable amount determined by the Contrast control. The board also processes the three signals with variable aperture correction (Detail control) and with DC restoration (Brightness control). Finally, a beam current limiter circuit lowers both the brightness level and the contrast level if a threshold beam current is exceeded.

The 2V p-p video signal at pin 1 is coupled by R1 and C1 to R2, one of the three sections of the Contrast control. From the Contrast control emitter follower Q1 buffers the signal into the aperture correction circuitry. However, note that Q1 is biased at its base by the 10V reference, and when the Normal-Service switch in the "service" position this bias is removed. In that case the voltage on Q1's emitter falls until it is clamped to 5.5V by D4, cutting off Q1, and thus the output of the board is determined entirely by the Brightness control, i.e., that circuitry after C7. In the aperture correction circuitry the signal voltage is coupled by R4 into two separate paths. R4, L1, and C4 act as a single section delay line which serves to introduce high-end group delay with respect to the signal that is coupled by C3 to Q3's base. The delayed signal is emitter-followed by Q2 to R10 and C5. Thus at the R10 end of Detail control R9 is a signal with essentially no aperture correction (and with a slight high frequency roll-off), and this represents the CCW position of the control. This same voltage is coupled by C5 to one end of R11, while the other end of R11 is the undelayed signal emitter-followed by Q3. Thus for those frequencies unaffected by R4, L1, and C4, the net voltage drop across R11 is zero, and consequently no current flows through R11 and Q3. (To ensure that there is no differential voltage at low frequencies it is necessary that the time constant involving C5 and R12 be closely matched to that involving C3 and the parallel combination of R7, R8, and Q3.) However, at higher frequencies the differential voltage across R11 increases and consequently a differential current flows through Q3 and R9. Thus, as the Detail control is rotated CW more of the differential voltage across R9 is added to the voltage on R10 (from Q2). This aperture-corrected signal with a variable amount of preshoot and overshoot is then applied to Q4's base and appears across R13.

The output of emitter follower Q4 is fed into C7, the clamp capacitor, where C7 and Q5 serve as the back porch clamp. The 30V back porch clamp pulse, timed to coincide with the back porch of each line of video, turns on field-effect transistor Q5, causing it to become a low value resistance; thus C26 is shorted to C7 and R16, and C7 charges or discharges rapidly. This action forces the voltage on the base of Q6 to be equal to the Brightness control voltage. When the back porch clamp pulse is over, Q5 opens up and the video is allowed to pass, but C7 has either charged or discharged to a new value depending on how much ripple or tilt previously existed on the incoming video. The back porch DC level is thus always maintained at exactly the Brightness control voltage. This process is known as DC restoration and/or backporch clamping. Note that the subjective brightness of the picture is determined by the *Contrast* control (on a TV which has DC restoration) because the Brightness control is used to set the brightness of picture elements that are near black, but the Contrast control determines the brightness of the white areas.

Q6 buffers the DC-restored signal to the output through drive control R19, which provides an AC gain adjustment. (See the video output board (1400) description for a more detailed explanation.) D2 and D3 together with Q26 and Q27 act as video clippers, since the output signal voltage can go no higher than two Vbe drops above Q26's base nor lower than two Vbe drops below Q27's base.

The brightness voltage on C26 for back porch clamping is fully available only if Q25 is "off". However, if anode sense current flowing in R80, R81, and pin 18 generates a voltage on Q24's emitter that exceeds D10's zener voltage, then Q24 saturates and quickly charges C30. C30 will continue to charge until Q25 turns on and draws current from the brightness circuit, thus reducing anode current. In the event of extremely excessive beam current C30 charges to D13's breakdown voltage, turning on Q28. This action lowers the White Limit Reference voltage until a safe amount of current is reached.

Fig. 1400-1